Remarks

Prior to entry of this Response, claims1-27 are pending in the application. This paper neither cancels nor adds any claims. Thus, following entry, claims 1-27 will remain pending.

1. Rejection Under 35 U.S.C. § 101

The Examiner rejected claims 2, 3 and 16 under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims 15 and 31 of U.S. Patent No. 6,228,730. The Applicant reserves the right to later file a terminal disclaimer to overcome this rejection, presuming no other grounds of rejection exist and claims 2, 3 and 16 remain pending in a form provoking the double patenting rejection.

2. Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 2-4, 16-21 and 25-27 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,623,628 to Brayton et al. (hereinafter "Brayton") in view of U.S. Patent No. 5,852,451 to Cox et al. (hereinafter "Cox"). Specifically, the Examiner alleged that Brayton teaches all limitations of these claims with the exception of "coupling the reordered requests to a texture memory," which the Examiner alleged is taught by Cox. For at least the following reasons, the Applicant respectfully disagrees with the Examiner's rejections.

Initially, and with respect to all claims, the Applicant respectfully submits one of ordinary skill in the art would not be motivated to combine Brayton and Cox. Brayton is generally directed to "ensuring consistency of data among various levels of caching in a multi-level hierarchical memory system" (see Abstract and col. 1, lines 63-66). Cox, by contrast, is directed to a system and method for improving bandwidth in a single memory "by improving memory locality in conventional page-mode memory systems" (Abstract and col. 3, lines 6-13). Thus, one of ordinary skill in the art would not look to Brayton and Cox in combination, because Brayton is not concerned with improving memory bandwidth and Cox is not concerned with data consistency throughout multiple memories.

Additionally, the combination of Brayton and Cox would be inoperable. Merely shoehorning Cox's Pixel Priority Heap (PPH) into Brayton would add no functionality to Brayton (and thus would not operate), insofar as the PPH has no ability to ensure data consistency. Likewise, adding the memory order buffer (MOB) or other elements of Brayton to the invention of Cox would be inoperable because Cox does not have multiple hierarchical levels of memory upon which Brayton's MOB may operate. Without a multi-level hierarchical memory, Brayton is

inoperable because the MOB cannot track load and store operations to the various memories. Thus, the combination of cited references cannot anticipate the inventions of claims 2-4, 16-21 and 25-27.

With the foregoing in mind, the rejections of individual claims are now discussed.

a. Independent claims 2 and 16

The Examiner alleged Brayton teaches all the limitations of claims 2 and 16 except for "coupling the reordered requests to a texture memory." The Applicant notes independent claims 2 and 16 have no such requirement. For at least the following reasons, the Applicant respectfully disagrees with the Examiner's rejections.

First, the Applicant notes independent claims 2 and 16 require "a memory control block... sequentially performing read operations on [a] memory system using... dispatched addresses." The Examiner makes no suggestion or teaching that either Brayton or Cox discloses a memory control block "sequentially performing read operations." The Examiner alleges Brayton's memory order buffer (MOB) is a memory control block. However, Brayton contains no teaching or suggestion that the MOB sequentially performs read operations, and the Examiner fails to cite any portion of Brayton as anticipating or suggesting this. Brayton's MOB blocks operations and stores information relating to the operation (such as "dependency information") (col. 11, lines 39-41). The MOB however, does not use an address to "sequentially perform read operations," as required by independent claims 2 and 16.

The load buffer 630 is part of the MOB (see col. 11, lines 35-37). Brayton explicitly teaches that the load buffer merely stores a LOAD operation for "re-dispatch," and transmits the operation when no conflict exists (col. 12, lines 39-42). The Applicant respectfully submits the MOB accordingly does not perform any read operations on a "memory system" using an address. Instead, it receives the results of a read operation, i.e., receives a LOAD micro-operation corresponding to a read operation (col. 10, lines 54-57) and passes the micro-operation on. It does not, however, perform the read operation in any way.

The Examiner further alleges Brayton's load buffer 630 teaches "a first-order queue" (Office action, page 3, line 8 of Fig. 4). Claims 2 and 16, however, requires a "first level *reorder* queue storing... current addresses" (emphasis added). Even presuming the Examiner meant that the load buffer 630 is a first level reorder queue, he provides no indication of how the load buffer 630 anticipates this limitation of independent claims 2 and 16. The Applicant notes "[t]he memory order buffer functions as a kind of *second-order* reservation station," not a "first level

reorder queue" (col. 11, lines 47-49). Without at least a suggestion as to how Brayton's load buffer 630 performs this function, the Examiner has not made a *prima facie* case of obviousness or anticipation.

The Examiner next alleges Brayton's load buffer 710 teaches an in-order tag queue, insofar as the load buffer tags each load operation "with the stored buffer ID of the store previous to it" (col. 14, lines 40-47).

Independent claims 2 and 16 require the in-order tag queue to store "first tag information, each piece of first tag information corresponding to an address in the first level reorder queue." That is, the information in the in-order tag queue must correspond to the information in the first level reorder queue. By contrast, Brayton's load buffer 710 stores only *store buffer* IDs. The Examiner has not alleged, nor does Brayton teach, that the load buffer 710 stores any form of Ids or information corresponding to the load buffer 630. Thus, since the Examiner alleges the load buffer 630 teaches the "first level reorder queue," Brayton *must* teach that the load buffer 710 stores some form of "first tag information" corresponding to the addresses in the load buffer, not the store buffer. Brayton contains no such teaching or suggestion. The information stored in Brayton's load buffer 710 cannot anticipate or render obvious "first tag information corresponding to an address in the first level reorder queue," as required by independent claims 2 and 16.

Independent claims 2 and 16 further require an "out-of-order tag queue storing second tag information." The Examiner has not cited any portion of Brayton or Cox as teaching or suggesting the out-of-order tag queue, or indeed any form of "second tag information." Accordingly, the Applicant respectfully submits claim 2 cannot be anticipated or rendered obvious by either Brayton or Cox, either alone or in combination, because neither reference teaches this limitation.

The Examiner next alleges the conflict detection circuit 1472 of Brayton teaches a "conflict detection block," as required by independent claim 2. The Applicant respectfully disagrees.

The Applicant notes independent claim 2's conflict detection block require interaction with the "plurality of current addresses" stored by the first level reorder queue (see limitation (6b)), the memory control block (see limitation (6c)), the first level reorder queue (see limitation (6d)), the conflict queue (see limitation (6e)), and so forth. There is no teaching or suggestion in Brayton that the conflict detection circuit 1472 interacts with any such queue. Indeed, Brayton neither teaches nor suggests that its conflict detection circuit 1472 writes to the alleged

equivalent of the first level reorder queue, the conflict queue, the in-order tag queue, or the out-of-order tag queue as required respectively by limitations (6d)-(6g) of independent claim 2. Brayton teaches only that the conflict detection circuit writes to the outbound queue circuit 1476, which in turn writes to the bus for transport presumably for ultimate writing to a main memory 421 (see col. 30, lines 9-31). By contrast, the load buffer 630 and MOB are part of the "memory subsystem" of a processor, not part of the main memory (col. 10, lines 11-13).

For at least the foregoing reasons, the combination of Brayton and Cox cannot anticipate or render obvious independent claims 2 and 16. Accordingly, the Applicant respectfully requests the Examiner withdraw his rejection and allow these claims over the cited references.

b. Independent claim 3

The Examiner has not specifically cited any portion of Brayton or Cox against the operations of the method recited in independent claim 3. For at least this reason, the Examiner has not established a *prima facie* case of obviousness. Accordingly, claim 3 should be allowed over the cited references.

To the extent the Examiner alleges the function of the cited elements of Brayton and Cox anticipate or render obvious the operations of claim 3, the Applicant responds as follows.

First, as set forth above with respect to independent claim 2, the Applicant respectfully submits the Examiner has failed to show either Brayton or Cox disclose any form of "first tag information" or "second tag information." Accordingly, neither reference can disclose "maintaining a list of first tag information" or "maintaining a list of second stag information." Both of these limitations are required by independent claim 3. Accordingly, neither reference may anticipate or render obvious independent claim 3.

Similarly, because neither Brayton nor Cox teach or suggest any form of first or second tag information (nor does the Examiner allege such teachings or suggestions), the references cannot anticipate or render obvious limitations such as "[under certain circumstances] adding... to the list of first tag information," "[under other circumstances] adding... to the list of second tag information," or "reassembling data... according to the first tag information and the second tag information." The Applicant notes each of these limitations is required by independent claim 3.

Accordingly, for at least the foregoing reasons, the combination of Brayton and Cox neither renders obvious nor anticipates the invention of independent claim 3. The Applicant therefore respectfully requests the Examiner withdraw his rejection and allow independent claim 3.

e. Dependent claims 4 and 17-27

The Examiner rejected the pending dependent claims under 35 U.S.C. § 103(a) as unpatentable over Brayton in view of Cox (for claims 4, 17-21 and 25-27) or under 35 U.S.C. § 103(a) as unpatentable over Brayton in view of Cox, further in view of U.S. Patent No. 5,778,245 to Papworth (for claims 22-24). For at least the following reason, the Applicant respectfully disagrees.

Each of the dependent claims depends from an independent claim previously shown to be patentable over the cited references. Accordingly, the dependent claims are themselves patentable. The Applicant makes this statement without reference to or waiving the independent bases of patentability within each dependent claim.

For at least the foregoing reason, the Applicant respectfully requests the Examiner withdraw his rejections and allow the dependent claims.

3. Conclusion

The Applicant thanks the Examiner for his careful review of the claims. The Applicant respectfully submits the present Response fully replies to the Office action and places the application in condition for further substantive review.

This paper is submitted on 20 September 2005 in response to the Office action mailed 20 April 2005. Accordingly, a two-month extension of time is necessary. Please treat this as a petition for such an extension and authorization to charge Deposit Account No. 04-1415 as necessary.

The Applicant believes no further petitions or fees are required. However, if any such are due, please treat this as a request therefor and authorization to charge the above-referenced Deposit Account as necessary.

If the Examiner should require any additional information or believes any further issues exist which may be solved by telephone, please contact the undersigned at (303) 629-3400.

Respectfully submitted,

Date: 20 September 2005

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